

gas with a small C/F ratio to] comprises a first amount of a first fluorocarbon gas with a large C/F ratio [are] mixed with a second amount of a second fluorocarbon gas with a small C/F ratio, the amount of said second fluorocarbon gas being equal to or less than the amount of said first fluorocarbon gas.

3. (Amended) Semiconductor device manufacturing method described in Claim 2 [where] wherein  $C_4F_8$  is used as the [aforementioned] first fluorocarbon gas and at least one selected from the group composed of  $CHF_3$ ,  $CH_2F_2$  and  $CF_4$  is used as the [aforementioned] second fluorocarbon gas.

4. (Amended) Semiconductor device manufacturing method described in Claim 1 [where] wherein the [aforementioned] insulating layer is plasma-etched with the [aforementioned] mixed gas of fluorocarbon gases.

5. (Amended) Semiconductor manufacturing device described in Claim 1 [where] wherein a lower conducting layer is formed on the [aforementioned] semiconductor substrate as an electrode or wiring, a connection hole is formed by [the aforementioned] etching [in] the [aforementioned] insulating layer that covers [this] the lower conducting layer, and an upper conducting layer [that is] connected to the [aforementioned] lower conducting layer is formed in the [aforementioned] connection hole as an electrode or wiring.

6. (Amended) Semiconductor device manufacturing method described in Claim 5 [where] wherein the [aforementioned] lower conducting layer has a titanium nitride layer on the surface where the [aforementioned] connection hole is formed and the [aforementioned] insulating layer includes a spin-on glass layer.

7. (Amended) Semiconductor device manufacturing method described in Claim 6 [where] wherein the [aforementioned] lower conducting layer is made of a stacked structure [where] having a titanium nitride layer, a layer of aluminum or an alloy thereof, a titanium layer, and a titanium nitride layer [are] stacked in that order, and the [aforementioned] insulating layer is made of a stacked structure [where] having a silicon oxide layer formed from tetraethyl/orthosilicate, a spin-on glass layer, and a silicon oxide layer formed from tetraethyl/orthosilicate [are] stacked in that order.

8. (Amended) Semiconductor device [in which] wherein a lower conducting layer [that has] having a titanium nitride layer on its surface is formed on the semiconductor substrate as an electrode or wiring, a connection hole is formed in an insulating layer that includes a spin-on glass layer to cover [this] the lower conducting layer, and an upper conducting layer [that] is connected to the [aforementioned] lower electrode layer [is] formed in the [aforementioned] connection hole as an electrode or wiring, [where] wherein the [aforementioned] connection hole [is] formed to the center position of the thickness of the [aforementioned] titanium nitride layer through the [aforementioned] insulating layer.

9. (Amended) Semiconductor device described in Claim 8 [where the aforementioned] wherein the lower conducting layer [is made of] comprising a stacked structure [where] having a titanium nitride layer, a layer of aluminum or an alloy thereof, a titanium layer, and a titanium nitride layer [are] stacked in that order, and the [aforementioned] insulating layer is made of a stacked structure [where] having a silicon oxide layer formed from tetraethyl orthosilicate, a spin-on glass layer, and a silicon oxide layer formed from tetraethyl orthosilicate [are] stacked in that order.